

# Photonic Integrated Circuits - Requirements on Integration & Assembly

# LIGENTEC

Leader in low loss Silicon Nitride Integrated Photonics



EPFL



LIGENTEC

European PIC Company

European origin



Europe based

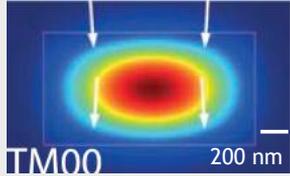


Global Reach



Headquarters in Lausanne (CH)  
Originating from EPFL (Kippenberg Lab)

## Thick SiN – the game changer



**90% of the light is confined**

- o Low propagation loss
- o Small chip size
- o Non-linear optics
- o High Power, VIS to IR

**All Nitride Core Technology:** combining the benefits of

- Silicon Nitride (VIS-IR, low loss, high power) with
- Silicon Photonics (small chip size, scalability)

## Versatile PIC Platform

**3+ thicknesses**

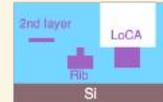
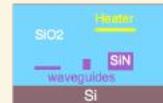
800 nm

400 nm

150 nm

custom

**10 process modules**



- o Modular
- o CMOS compatible
- o Scalable

**Extensive PDK**

**Design rules**

**Design Rule Checks**

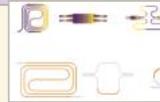
**Layout files**

**Primitives**

**Building Blocks**

**IP Cores**

- Components**
- Waveguides, delay lines
  - Couplers / MMIs
  - Crossings
  - Filters (RRs, AWGs)
  - Switches
  - Polarization mgt
- Optical I/O**
- Grating couplers
  - Inverted tapers
  - Spot size converters



**Design flows**

VLC PHOTONICS  
Mentor  
SYNOPSIS  
LUCEDA  
XyPhotonics  
ANSYS

- Simulations**
- Component and circuit simulation
  - Technology files
  - Cross section

## Commercial Offering

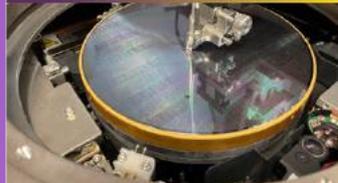
**R&D and Prototyping**

*Open access, low barrier*



**Custom PIC Developments**

*High flexibility & competence*

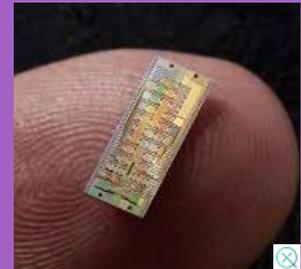


**Manufacturing**

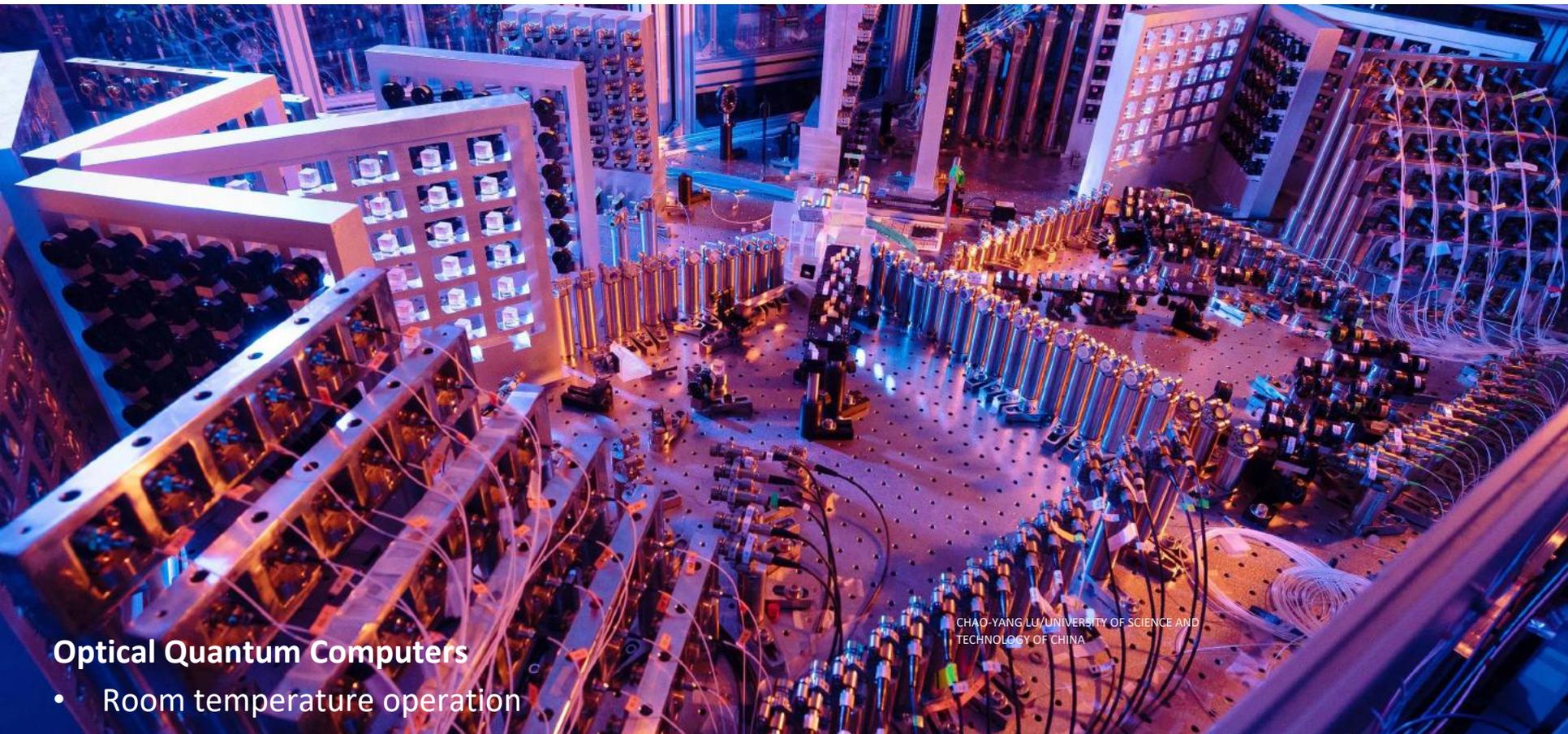
*Niche to high volumes*



## We deliver PICs



*Do we really need Photonic Integration?*  
**Use case: Quantum Computing**



**Optical Quantum Computers**

- Room temperature operation

CHAO-YANG LU/UNIVERSITY OF SCIENCE AND  
TECHNOLOGY OF CHINA

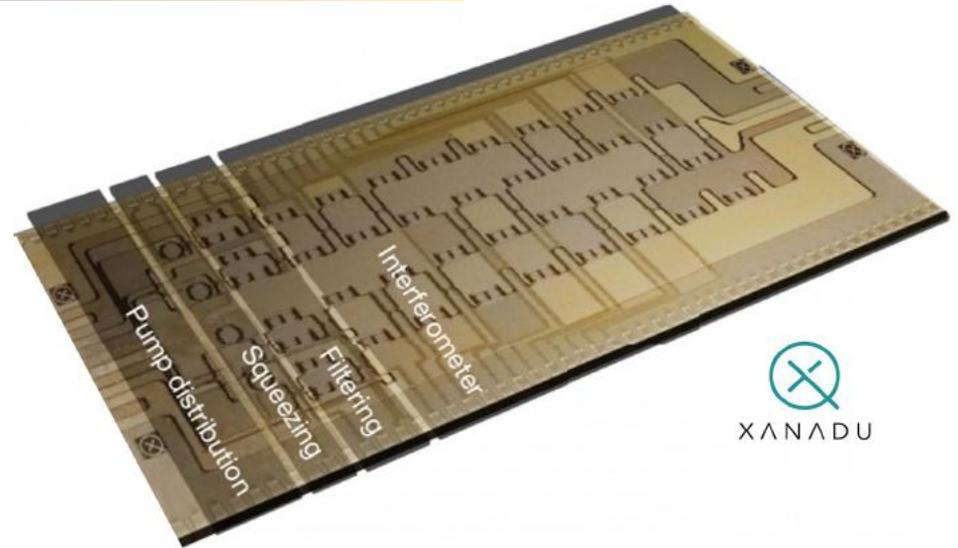
# Do we really need Photonic Integration?

## Use case: Quantum Computing



### Optical Quantum Computers

- Room temperature operation
- **Not scalable with discrete optics!**



### PIC based Photonic Quantum Computers

- Scalable with existing, semiconductor like manufacturing technologies

# Problem - Barriers for Breakthrough Photonic Integrated Circuits (PICs) ...

... have a huge potential



## Disruptive PICs:

Size: 100x smaller

Weight: 100x lighter

Power: 1/10<sup>th</sup> of energy consumption

Cost: 1/100<sup>th</sup> of cost

To repeat the electronic IC revolution.

... and have become technology of choice in  
selected markets,

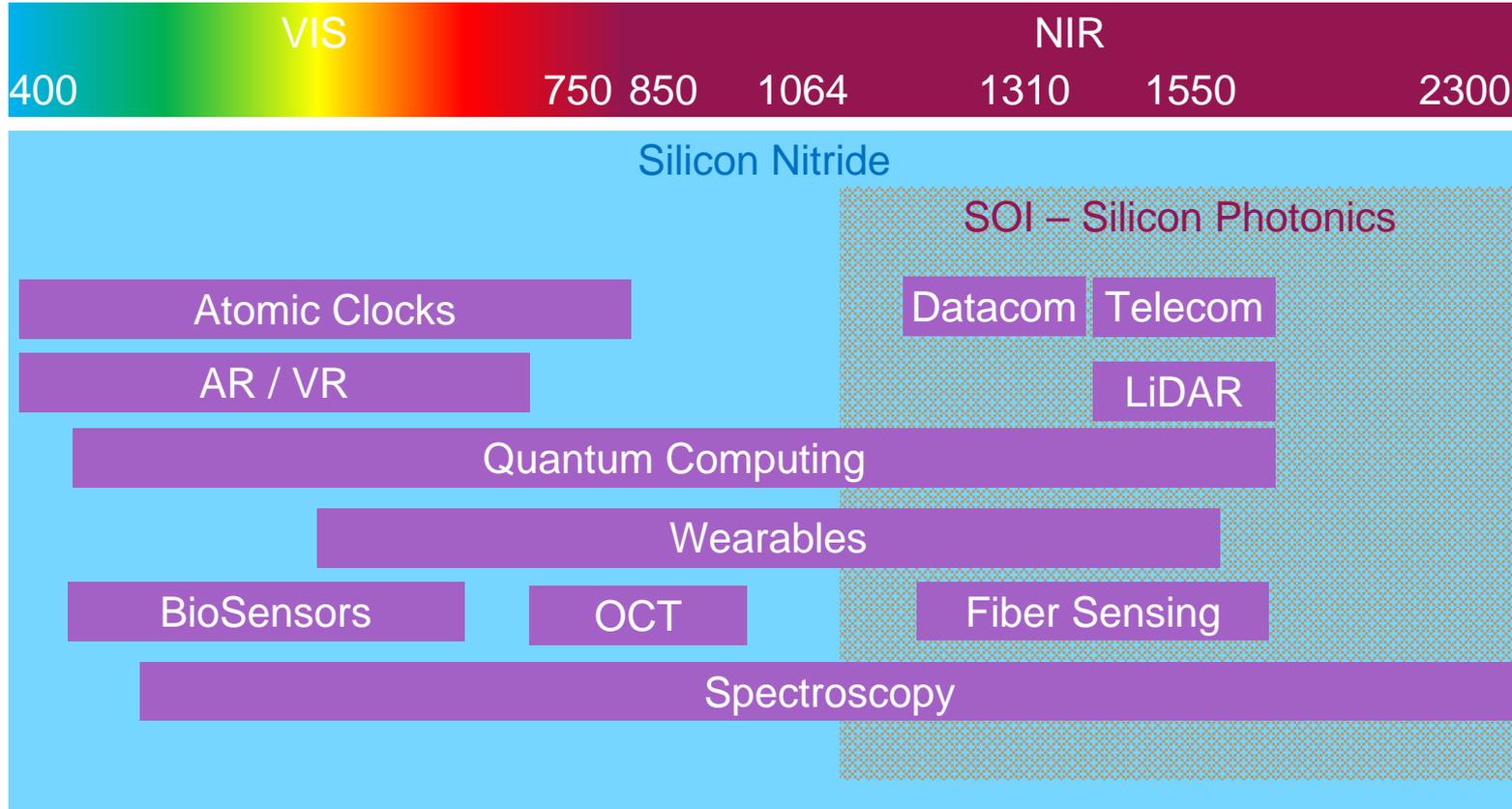


but larger scale adoption



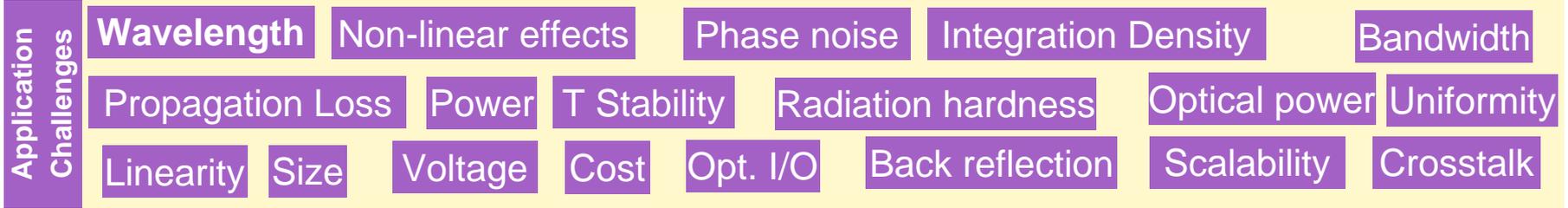
is still challenged by:

- ❑ On chip and in/out coupling losses
- ❑ Long & expensive R&D cycles
- ❑ No one fits all solution



# Challenge application diversity

## Combine the best



	InP	Silicon	SiN	Silica
<b>Wavelength</b>	NIR upwards	NIR to MIR	VIS to MIR	VIS to MIR
<b>Passives</b>	Low loss	Moderate loss, TPA, T sensitive	Very low loss, high power	Very low loss
<b>Lasers</b>	Monolithic	Monolithic / heterogeneous	Heterogeneous integration	External / hybrid
<b>Modulators</b>	Monolithic	Monolithic / heterogeneous	Heterogeneous integration	NA
<b>Photodetectors</b>	Monolithic	Monolithic	Monolithic / heterogeneous	External / hybrid
<b>Compactness / index contrast</b>	low	high	moderate	high
<b>Cost</b>	High	Low	Low	High
<b>Maturity</b>	high	high	emerging	high

There is **no** one fits all technology

High application diversity, no one fits all solution, Optimizing for a single application only possible high-volume applications

### Approach:

Best and scalable base platform for circuitry with standard I/Os and PDK



Application specific choices of integration

⇒ Combine the best to lower adoption barriers

*One basis, large diversity in the add-ons*  
**Materials and Functionalities**

**Use SiN as base platform for general circuitry**

- Comprehensive PDK
- Standard I/Os
- Scalable to volume

**Add-on Functionalities for Light**

- Generation
- Modulation
- Amplification
- Detection

Many great materials, each comes with their own merits (and challenges):

InP

GaAIAs

BTO

Plasmonics

Polymer

LNO

AlN

...

SiN

SiO<sub>2</sub>

SiN

SiN

Si

## Monolithic Integration

*Deposited or grown on the wafer*

- Best cost option
- Limited material choice

InP  
PICs

SOI  
Modulators

## Heterogeneous Integration

*Transferred / bonded on the wafer*

- High flexibility
- Low cost potential

Wafer to wafer

Chip to wafer

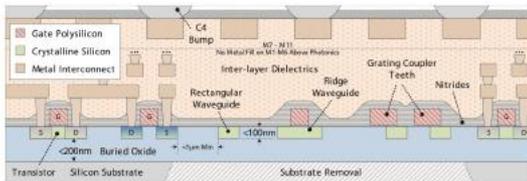
uTP

## Hybrid Integration

*Assembled in the package*

- High flexibility
- Costly in volumes

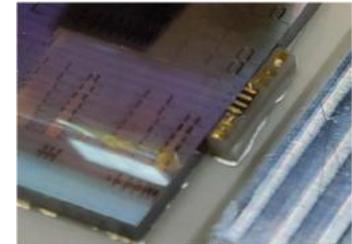
Butt coupled PDs



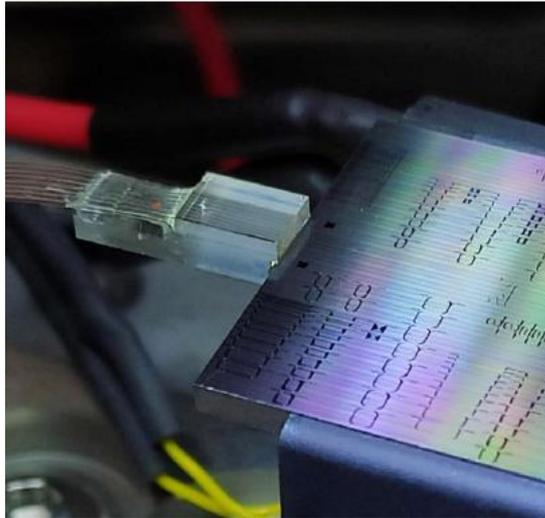
Sun et al., JSSC, 50, 893 (2016)



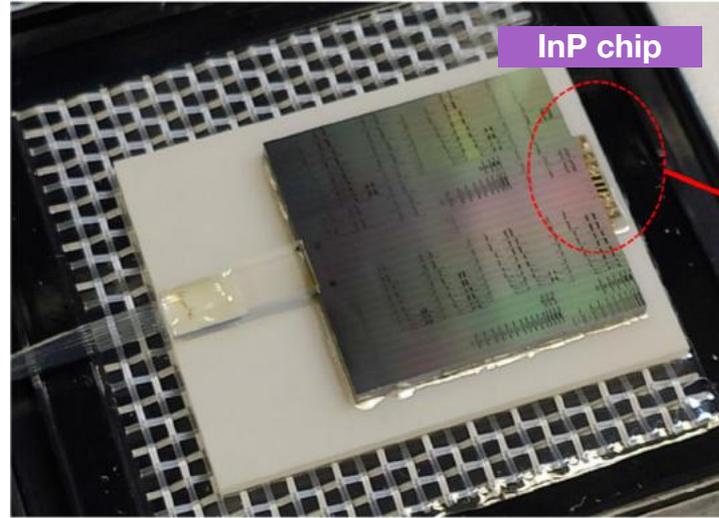
Source: EVG



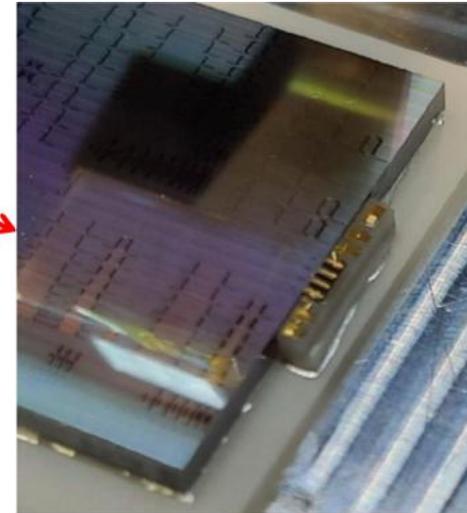
*Hybrid Integration – edge coupled*  
**Fiber coupled passive SiN Chip with InP Chip attached**



Fiber Array to SiN waveguides



Glued on carrier



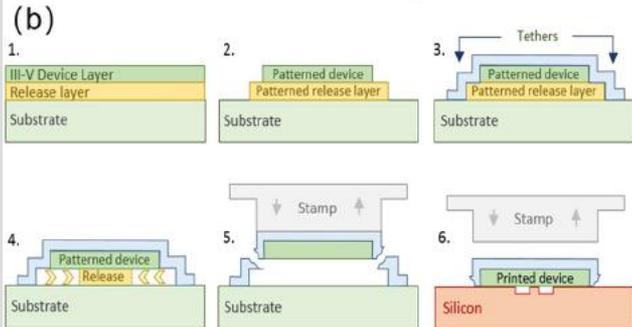
III-V Chip attached to SiN PIC

# Heterogeneous Integration – Chip to Wafer Example

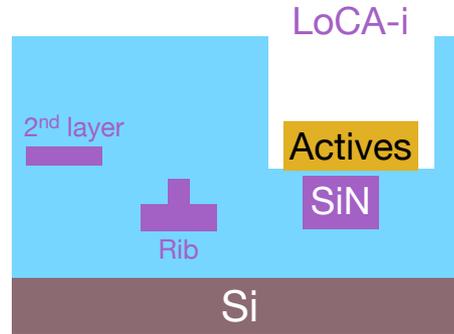
## Micro-Transfer Printing



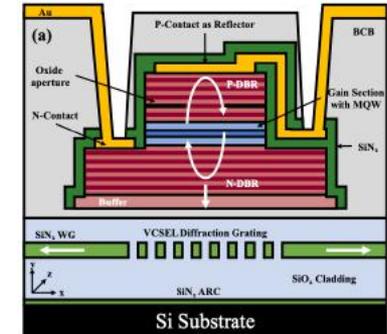
### Micro Transfer Printing Technology



Roelkens *et al.*, in *2018 IEEE Optical Interconnects Conference (OI)* (IEEE, USA, 2018), pp. 13–14.



### Example VCSEL on SiN PICs



Goyvaerts *et al.* 2021, *Optica* 8, 1573-1580 (2021)

### Micro Transfer Printing:

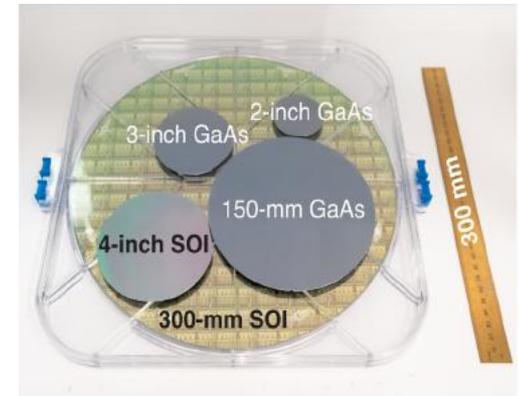
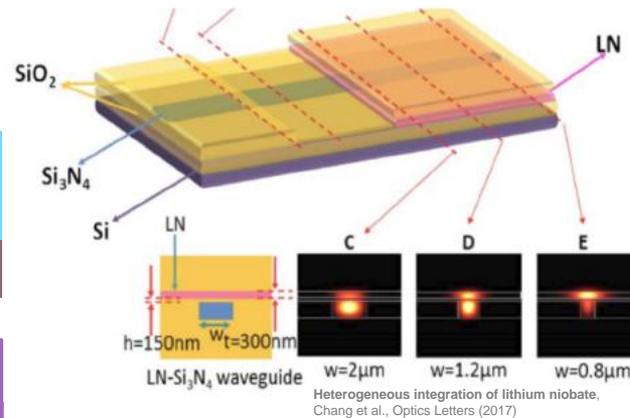
- Wide range of materials / components
- Cost effective, on-wafer processing
- Highly efficient usage of source material
- Great for the integration of III-V materials (lasers, modulators, amplifiers, modulators, detectors)
- Match of different components / materials on one wafer
- **Requires specially engineered source Epi stacks**

# Heterogeneous Integration – example Wafer to Wafer

## Thin Film Lithium Niobate on SiN



Thin Film LNOI bonded  
on SiN PIC wafer

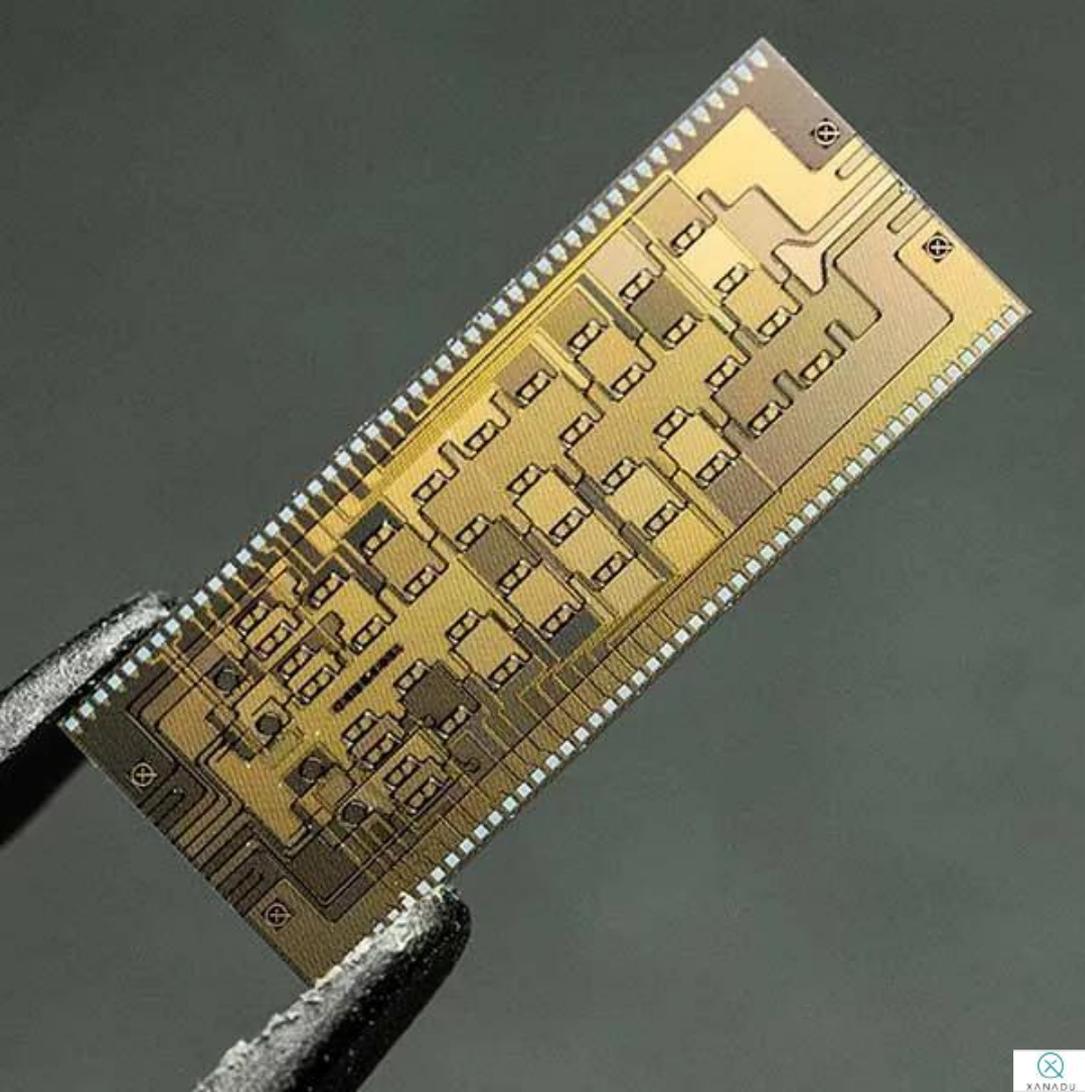


### Key Benefit

- Lithography replaces mechanical positioning

### Key Challenges

- Yield of combined stack
- Wafer size compatibility
- Source wafer utilization



**PICs are  
useless,**



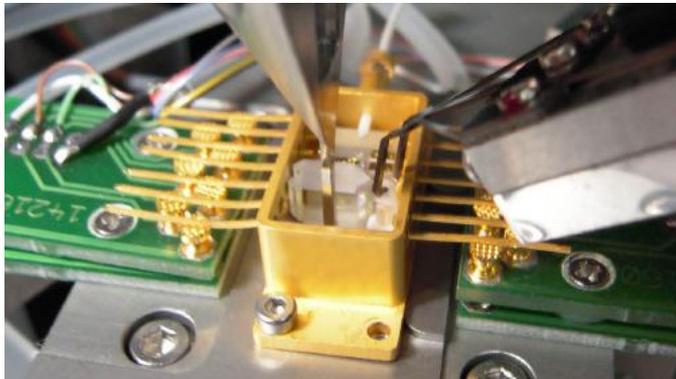
PICs are  
useless,  
unless they  
are  
packaged!

### Electrical Connections

- Critical for high frequencies (>10GHz)

### Housing / encapsulation / stabilization

- Hermetic packaging
- Thermal stabilization
- ....



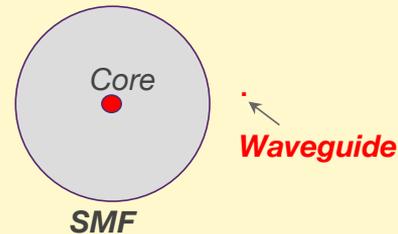
### Optical Connections

- Important source of loss: 1dB (20%) to 6dB (65%) loss per coupling

### Problem statement:

Mode mismatch, very different to electrical connections.  
Sub um accuracies required.

Fiber mode (10 um) >>  
waveguide mode (2-3 um)



**Decrease**  
fiber mode

or

**Enlarge**  
waveguide mode

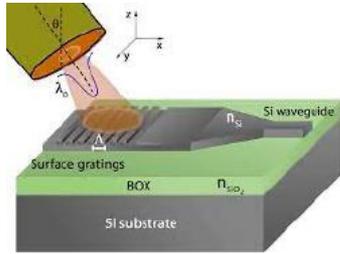
# Solutions Strategies

## Fiber to Waveguide Coupling Strategies

### Vertical

#### Grating couplers

- (+) wafer level testing
- (+) wafer level integr.
- (-) bandwidth
- (-) lossy

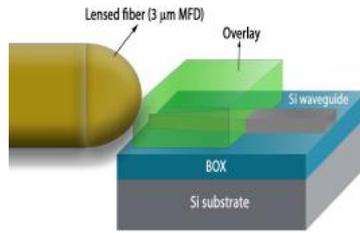


*Appl. Sci.* **2018**, *8*, 1142; doi:10.3390/app8071142

### Edge

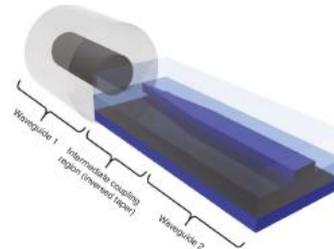
#### Reduce Fiber mode

- High NA Fiber
- Lensed fibers
- (+) coupling
- (-) alignment
- (-) expensive



#### On chip expansion

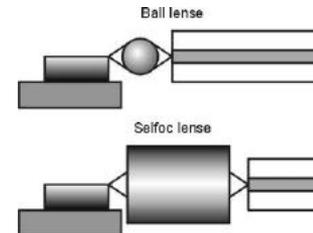
- Inverted tapers
- (+) coupling
- (+) alignment
- (+) standard SMF



*Nanophotonics* 2018; 7(12): 1845–1864

#### Free space

- (+) coupling
- (+) alignment
- (-) expensive



DOI: 10.5772/51626

#### Photonic wirebonds

- (+) Chip to Chip
- (o) experimental

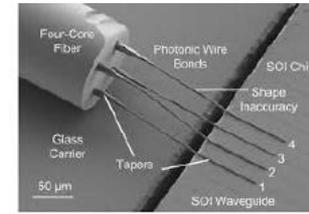
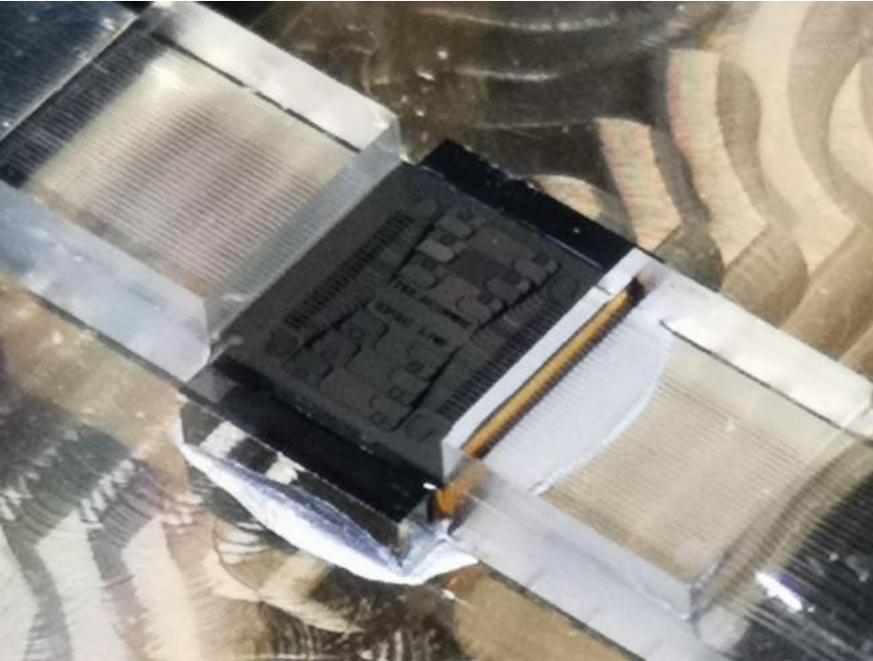


Fig. 8: Fabricated example: Photonic wire bonds (DWBs) connect the

DOI:10.1109/OIC.2014.6886114

*Mode Size expansion helps*  
**Optical I/O – there is more**

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**Challenges:**

- Mode matching
- Reflections, facet quality
- Materials
- Aging, shrinkage
- Tolerances
- **Low cost at high precision**
- **High Mix - Low Volumes**
- Missing standards

**Requires**

- Sophisticated mode expanders
- Design for assembly
- Close interaction PIC designer, foundry, packaging house and equipment manufacturer

## Integration

- **Photonic Integration** needed & **disruptive**
- Requires use of **different technologies**
- **Wafer scale** integration preferred choice

## Assembly

- Higher complexity than electronics
- Small mode fields of waveguides makes **assembly expensive**
- **Mode expansion** for cost reduction
- Use **standardization**

Swiss PIC industry needs **local expertise** in assembly & packaging to leverage existing strength in chip technologies.

# Thanks to the Ligentec Team

**Join our PIC journey!**

check out our openings at [ligentec.com/careers](https://ligentec.com/careers)  
or send your CV to [hr@ligentec.com](mailto:hr@ligentec.com)